

FIG. 1

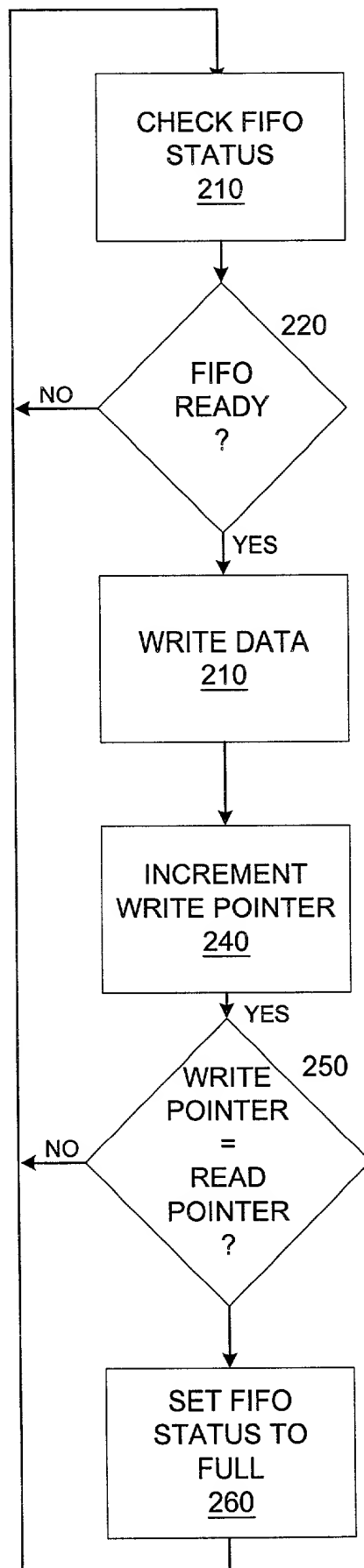


FIG. 2

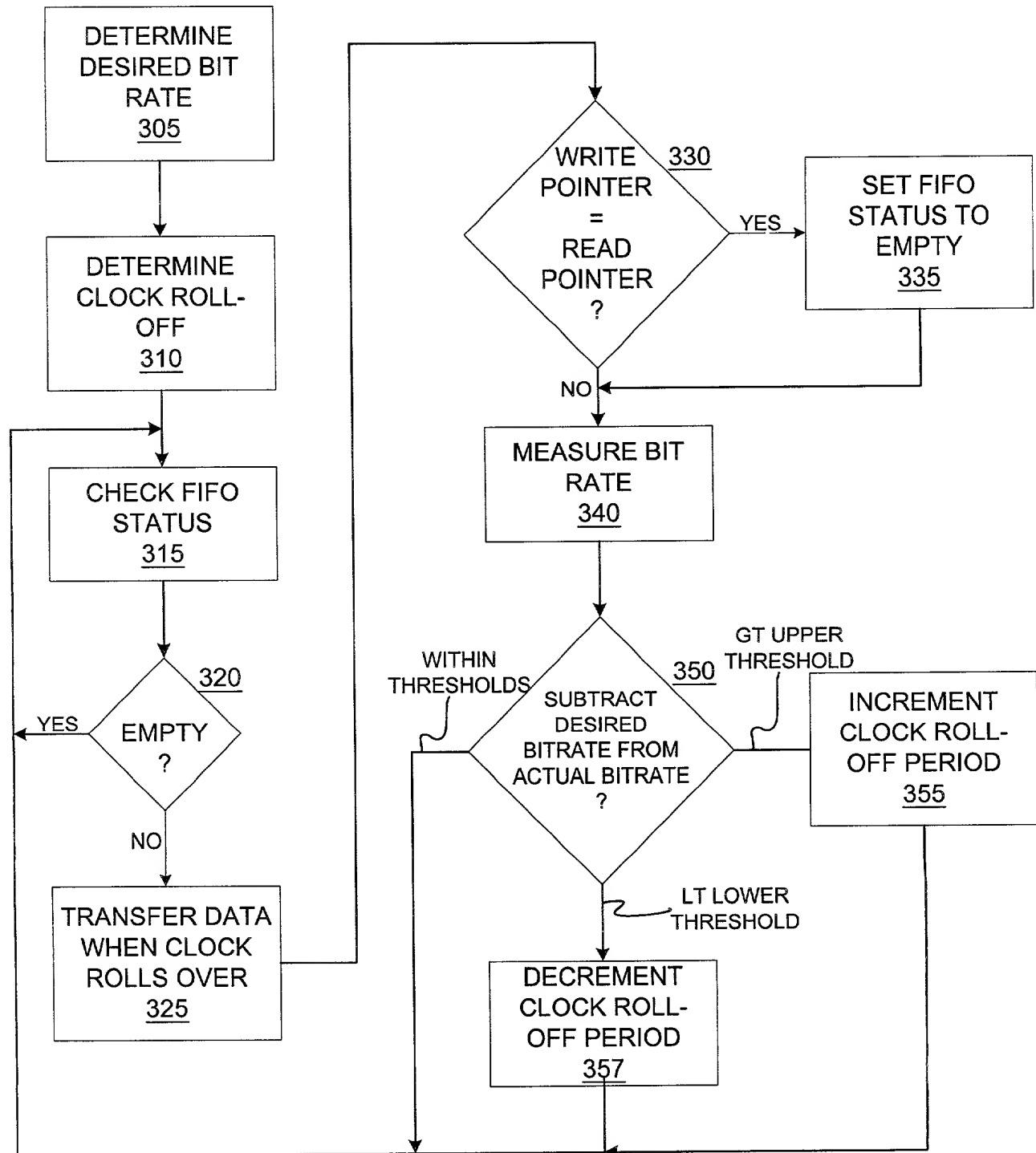


FIG. 3

| TD_DATA_CNTL - RW - | | | |
|-----------------------|-------|---------|---|
| Field Name | Bits | Default | Description |
| TD_REG_DATA_MODE | 0:1 | '00' | 0= normal operation, 1= register input mode. 2= bus mastered input mode. 3= reserved. |
| TD_DATA_RDY | 2 | '0' | Read only. Software has to check this field for next register write. Otherwise, data would be overwritten and corrupted. |
| TD_SYNC_LOST | 12 | '0' | read only . 0= normal operation, 1= data was overwritten. |
| TD_DATA - RW | | | |
| Field Name | Bits | Default | Description |
| TD_DATA | 31:0 | 0x0 | |
| TD_BM_MACRO_CNTL - RW | | | |
| Field Name | Bits | Default | Description |
| TD_BM_RST | 0 | 0x0 | 0= no reset , 1= reset all pointers. |
| TD_BM_LOCK | 1 | 0x0 | 0= normal operation, 1= lock the internal FIFO. |
| TD_BM_DEBUG | 2 | 0x0 | 0= normal operation, 1= snoop into the FIFO (after locking). |
| TD_BM_LEAK_RATE | 15:8 | 0x6 | Control the data consumption from the BM FIFO read side. The value is in terms of MCLK cycles (GUI clock of 75MHz) between bytes. |
| TD_BM_ADDR | 21:16 | 0x0 | BM FIFO address, in lock and debug modes. |
| TD_BM_MACRO_DATA - RW | | | |
| Field Name | Bits | Default | Description |
| TD_BM_MACRO_DATA | 31:0 | 0x0 | |

FIG. 4